

Appl. No. 09/751,427  
Amdt. dated February 10, 2004  
Reply to Office Action of December 10, 2003

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (currently amended):

An apparatus comprising:

a configurable link which permits

a first level of access if couples a computer's central processing unit (CPU) to a bus as a default bus master and couples a first peripheral device to the bus as a slave device if the computer's CPU is in a first power management state; and

a second level of access couples the first peripheral device to the bus as the default bus master if the computer's CPU is in a second power management state.

2. (original):

The device of claim 1, wherein the first power management state and the second power management state each comprises a set of power management states.

3. (currently amended):

The apparatus of claim 1, ~~wherein: further comprising:~~

~~a the first peripheral device communicatively coupled to the configurable link wherein the first level of access the peripheral device is capable of operating as a conventional peripheral device when coupled to the bus as the slave device.~~

4. (currently amended):

The apparatus of claim 1, ~~wherein: further comprising:~~

~~a the first peripheral device communicatively coupled to the configurable link wherein the second level of access the peripheral device is capable of operating as the default bus master for the computer without assistance from the CPU.~~

5. (currently amended):

The apparatus of claim 4, wherein ~~a the first peripheral device coupled to the configurable link causes the configurable link to couple the first peripheral device to the bus as the default bus master operate in the second level of access~~ when the CPU is in a second power management state.

6. (previously presented):

The apparatus of claim 1, wherein the computer's CPU is in a sleeping state in the second power management state.

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## 7. (original):

The apparatus of claim 1, wherein the second power management state includes power modes S3-S5 as defined in the Advanced Configuration and Power Interface (ACPI) specification.

## 8. (currently amended):

The apparatus of claim 1, wherein the transfer rate over the configurable link when the first peripheral device is the default bus master in the second level of access is different than when the computer's CPU is the default bus master in the first level of access.

## 9. (currently amended):

The apparatus of claim 1, further comprising:

- a first peripheral device coupled to the configurable link; and  
an input/output hub communicatively coupling the configurable link and the central processing unit (CPU).

## 10. (currently amended):

The apparatus of claim 9, wherein the CPU manages the input/output hub to control communications to and from the first peripheral device when the computer's CPU is the default bus master in the first level of access.

## 11. (currently amended):

The apparatus of claim 9, wherein the configurable link enables the first peripheral device to manage the input/output hub to control communications to and from the first peripheral device when the first peripheral device is the default bus master in the second level of access.

## 12. (original):

The apparatus of claim 9, further comprising

- a second peripheral device communicatively coupled to the input/output hub.

## 13. (currently amended):

The apparatus of claim 12, wherein the first peripheral device can communicate directly with the second peripheral device without assistance from the CPU when the first peripheral device is the default bus master in the second level of access.

## 14. (currently amended):

A method comprising:

- configuring a link to provide a first level of access to couple a computer's central processing unit (CPU) to a bus as a default bus master and couples a first peripheral device to the bus as a slave device ~~resources~~ if the computer's central processing unit (CPU) is in a first power management state; and

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configuring the link to ~~provide a second level of access to the computer's resources~~  
couple the first peripheral device to the bus as the default bus master if the computer's  
CPU is in a second power management state.

## 15. (currently amended):

The method of claim 14, ~~wherein further comprising: coupling a peripheral device to the~~  
~~configurable link wherein the second level of access~~ the first peripheral device is capable of  
operating as the default bus master for the computer without assistance from the CPU.  
~~computer.~~

## 16. (currently amended):

The method of claim 15, wherein the first peripheral is capable of operating as a conventional  
peripheral device when coupled to the bus as the slave device. ~~in the first level of access.~~

## 17. (previously presented):

The method of claim 14, wherein the computer's CPU is in a sleeping state in the second  
power management state.

## 18. (original):

The method of claim 14, wherein the second power management state includes power modes  
S3-S5 as defined in the Advanced Configuration and Power Interface (ACPI) specification.

## 19. (currently amended):

The method of claim 14, wherein ~~a~~ the first peripheral device coupled to the configurable  
~~link causes the configurable link to couple the first peripheral device to the bus as the default  
bus master operate in the second level of access when the CPU is in a second power  
management state.~~

## 20. (currently amended):

The method of claim 14, wherein configuring the link to couple the first peripheral device to  
the bus as the default bus master ~~provide a second level of access~~ also requires configuring  
an input/output hub to which the link couples to allow the peripheral device to become the  
default bus master.

## 21. (currently amended):

A system, comprising:

a sub-system to detect the power management state of a central processor;

a sub-system to determine whether the central processor is in a first power management  
state or a second power management state;

a sub-system to couple allow the central processor to a bus as a default bus master and to  
couple a first peripheral device to the bus as a slave device ~~manage data flow over an~~  
~~input/output hub~~ if the central processor is in a first power management state; and

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a sub-system to ~~couple the~~ configure a link coupling the input/output hub to a first peripheral device to the bus as the default bus master to allow the first peripheral device to manage data flow over the hub if the central processor is in a second power management state.

22. (original):

The system of claim 21, further comprising:

a sub-system to initiate a data transfer from the first peripheral device if the central processor is in the second power management state.

23. (original):

The system of claim 21, further comprising:

a sub-system to buffer data at the first peripheral device if the central processor is in the second power management state.

24. (original):

The system of claim 21, further comprising:

a sub-system to allow the first peripheral device to directly access and communicate with a second peripheral device without assistance from the central processor.

25. (original):

The system of claim 21, further comprising:

a sub-system to delay the central processor from transitioning from the second power management state to the first power management state.